REMARKS

The Examiner's Action mailed on September 11, 2006, has been received and its contents carefully considered. Additionally attached to this Amendment is a Petition for Extension of Time, extending the period for response to January 11, 2007.

In this Amendment, Applicant has amended claims 1 and 10, has canceled claims 9, 12 and 15, and has added claims 16 and 17. Claims 1-8, 10-11, 13-14, and 16-17 are pending in the application, while claims 2-8 and 11, 13-14 are withdrawn from consideration. Claims 1 and 16 are the independent claims. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner's Action rejects claims 1 and 10 as being obvious over *Ogawa* (USP 4,418, 284) in view of *Hashimoto* (USP 6,333,565). It is respectfully submitted that the invention now defined by these claims is clearly patentable over the cited references for at least the following reasons.

Amended claim 1 is directed to a semiconductor device having a constitution which is simplified in comparison with a conventional device. Applicant's claimed invention achieves this and other purposes by providing 'an insulating film provided over a main surface of a semiconductor chip and surrounding side surfaces of first pads,' 'a wiring patterns extending over the insulating film,' 'post portions provided on and electrically connected to the wiring patterns,' and 'external terminals provided on the post portions.' The advantages of this configuration are discussed, for example, throughout Applicant's specification. This claimed invention is not disclosed, suggested, or taught by the cited references.

Ogawa discloses a solid-state color-image sensor with a light-shield layer covering desired portions so as to prevent noise. However, as is noted by the Examiner, *Ogawa* does not disclose or suggest post portions, the wiring layer electrically connected to the post portions, and the external terminals provided on the post portions, as recited in claim 1.

Moreover, *Ogawa* teaches away from the external terminals recited by claim 1. *Ogawa* does not disclose any external terminals provided on the solid-state color-image sensor. Instead, *Ogawa* discloses the pads 6 are outside the resin layer 13 or the pads 113 are outside the adhesive layer 130 (see *Ogawa* Figures 3 and 15). This is similar to Applicant's admitted prior art, and implies that the external terminals are located beyond the image sensor. When external terminals, such as solder balls, are not provided in the image sensor, such an image sensor uses a conventional wire bonding method (see Applicant's specification page 2, lines 2-4). Accordingly, *Ogawa* discourages one of skill in the art from fabricating the external terminals in the image sensor, as recited by claim 1.

To overcome the above admitted deficiencies, the Examiner relies on the teachings from *Hashimoto*. *Hashimoto* discloses a semiconductor device which is a CSP type with a package size approximately equal to a semiconductor chip. However, *Hashimoto* does not disclose or suggest the insulation layer, the wiring layer, the post portions, and the external terminals, as recited in claim 1.

Hashimoto teaches providing a depression 16a in an intermediate layer 16, which may be a space or be filled with a flexible resin 32 (see *Hashimoto* Col . 7, lines 31-33, Figure 1 and Col. 9, lines 24-29, Figure 4). However, neither the depression 16a

nor the intermediate layer 16 are not equivalent to the insulating film defined by amended claim 1. It is because neither the depression 16a nor the intermediate layer 16 surround the electrode 14 while the insulating film as recited in claim 1 surrounds and contacts side surfaces of the first pads.

Further, the conductive foil 22 disclosed in *Hashimoto* is not equivalent to the wiring patterns, as recited by claim 1. The conductive foil 22 is formed to be larger than the opening outline of the depression 16a and is disposed so as to cover the depression 16a (see Col. 6, lines 61-64, Figure 1). In other words, the conductive foil 22 is partially supported by the intermediate layer 16 and has the depression 16a underneath so as to easily deform, thereby easily absorbing the stress applied the external electrode 26 (Col. 7, lines 31-13). On the contrary, the wiring patterns defined by amended claim 1 extend over the insulating film that surrounds the first pads. It is thus noted that the conductive foil 22 is a different feature from the wiring patterns recited by claim 1.

Neither does *Hashimoto* teach the post portions defined in amended claim 1. *Hashimoto* discloses that the electrode 26 is formed on the conductive foil 22 so as to extend through the penetrating hole 20a (see *Hashimoto* Col. 7, lines 12-16, Figure 1). However, the portion of the external electrode 26, which is formed in the penetrating hole 20a, is not equivalent to the post portions, as recited by claim 1. The depression 16a is formed in a region including immediately under the external electrode 26, while the insulating film recited by claim 1 is formed underneath the wiring patterns, thereby being formed underneath the post portions.

Further, the external terminal electrode 26 in *Hashimoto* is not equivalent to the external terminals recited by claim 1. The external electrode 26, as disclosed by *Hashimoto*, is formed on the conductive foil 22, while the external terminals defined in claim 1 provided on the post portions.

Furthermore, *Hashimoto* teaches away from the claimed invention. The statement in *Hashimoto* that 'a gap is formed between a substrate having external electrodes and a semiconductor chip' discourages one of skill in the art from fabricating an insulating film on the main surface of the semiconductor chip and surrounding side surfaces of the first pads. (see *Hashimoto* Col. 1, lines 23-28). It is noted that such a gap or depression 16a is a necessary element in *Hashimoto* to absorb the stress applied to the external electrode 26.

Accordingly, *Hashimoto* fails to disclose or suggest the insulating film, the wiring layer, the post portions, and the external terminals, as recited in claim 1.

It is thus submitted that Applicant's independent claim 1 is *prima facie* patentably distinguishable over the cited references.

The Examiner's Action also rejects claim 10, as being obvious over *Ogawa* in view of *Hashimoto*, and further in view of *Lanford* (USP 5,959,358). Because *Lanford* does not overcome the above-noted deficiencies of *Ogawa* and *Hashimoto*, and because claim 10 depends from independent claim 1, it is submitted that claim 10 is *prima facie* patentably distinguishable over the cited references for at least the same reasons as independent claim 1, as well as for the additional features recited therein. It is requested that claim 10 be allowed and that this rejection be withdrawn.

New claims 16 and 17 also recite an insulating film, a wiring pattern over the insulating film, a post electrode formed on the wiring pattern, and an external terminal formed on a top surface of the post electrode, and are allowable for at least the same reasons as independent claim 1, as well as for the additional features recited therein.

It is thus submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

Robert H. Berdo, Jr.
Registration No. 38,075
RABIN & BERDO, PC
Customer No. 23995
Telephone: 202-371-8976
Facsimile: 202-408-0924

RHB/JJ